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For: METHOD OF MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT
USING A SELECTIVE DISPOSABLE SPACER TECHNIQUE AND SEMICONDUCTOR
INTEGRATED CIRCUIT MANUFACTURED THEREBY

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

<u>Exam</u> <u>Init</u>	<u>Ref</u>	<u>Document</u> <u>Number</u>	<u>Issue</u> <u>Date</u>	<u>Name</u>	<u>Class</u>	<u>Sub</u> <u>Class</u>
_____	_____	6,043,537	3/28/2000	Jun, et al.		

Examiner: _____

Date Considered: _____